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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,003	02/05/2001	David Baker	655-0012c	5644

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EXAMINER
NGUYEN, TANH Q

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,003	BAKER ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/25/02 and 01/ 13/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/13/03 has been entered.

Specification

2. The amendment filed 05/09/02 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: a cache memory directly coupled to said first host processor system, said second local processor and said data transfer switch (recited in claim 37).

The original disclosure teaches the first **host** processor system being connected to the PCI/AGP buses (page 15, lines 7-14), the PCI/AGP interface [130, FIG. 1A], the data transfer switch [112, FIG. 1A] before being connected to the cache memory [110, FIG. 1A], hence does not teach the cache memory being directly coupled to the first **host** processor system. The original disclosure also teaches CPU C0, CPU C1, and FFU [102, 104, 106, FIG. 1A] being processors disposed within the multimedia

processor, hence are local processors and, therefore, do not constitute a first host processor system coupled to said multimedia processor (see claim 19, line 3).

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 37 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, the original disclosure teaches the first host processor system being connected to the PCI/AGP buses (page 15, lines 7-14), the PCI/AGP interface [130, FIG. 1A], the data transfer switch [112, FIG. 1A] before being connected to the cache memory [110, FIG. 1A], hence does not teach the cache memory being directly coupled to the first host processor system. The original disclosure also teaches CPU C0, CPU C1, and FFU [102, 104, 106, FIG. 1A] being processors disposed within the multimedia processor, hence are local processors and, therefore, do not constitute a first host processor system coupled to said multimedia processor (see claim 19, line 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 19-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Reader et al. (U. S. Pat. No. 6,192,073)** in view of **Kim (U.S. Pat. No. 5,926,187)**, and further in view of **Kusters (U. S. Pat. No. 5,519,112)**.

7. As per claim 19, **Reader et al.** (Reader) teaches an integrated multimedia system [100, FIG. 1] having a multimedia processor [110, FIG.1/FIG.2] disposed in an integrated circuit, said system comprising:

a first host processor system coupled to said multimedia processor (col. 3, lines 25-26);

a second local processor [210, 220, FIG.2] disposed within said multimedia processor for controlling the operation of said multimedia processor (col. 5, lines 1-3);

a cache subsystem [230, FIG. 2] disposed within said multimedia processor and coupled to said second processor for transferring data in said multimedia processor;

a data streamer [245, FIG. 2 and FIG. 3] coupled to said cache subsystem, and configured to schedule simultaneous data transfers among a plurality of modules [, 210, 220, 242, 243, 245, 248, 252, 255, 258, 290, FIG.2] disposed within said multimedia

processor in accordance with corresponding channel allocations (col. 4, lines 34-49; 8 channels, FIG. 52);

an interface unit [FBUS INTERFACE BLOCK, ASIC GLUE LOGIC AND DMA CONTROLLER, FIG. 52; MULTIMEDIA LIBRARY MODULE, FIG. 7] coupled to said data streamer [WDM Streaming Media, FIG. 7] having a plurality of I/O device driver units [MULTIMEDIA LIBRARY MODULE (MPEG, MODEM, AUDIO,...), FIG. 7]; and

a plurality of external I/O devices [KS0122, KS0119, AD1843, FIGs. 6 and 52] coupled to said multimedia processor.

Reader also teaches the data streamer receiving the output of VP [220, FIG. 2] and the VP receiving the output of the data streamer (col. 5, lines 11-13; col. 5, lines 29-30); and the scalar processor [210, FIG. 2] receiving the output of the data streamer (col. 5, lines 15-16) and the data streamer receiving the output of the scalar processor (col. 5, lines 23-27), therefore teaches simultaneous transfers between the data streamer and the scalar processor, and between the data streamer and the VP, through the cache subsystem memory.

Kim teaches a multimedia processor [200, FIG. 2] that is similar to Reader's multimedia processor [110, FIG. 2]; and in particular, the components of the cache subsystem [230, FIG. 2] comprising a control circuit [280, FIG. 2], a ROM cache [270, FIG. 2], data caches [264, 268, FIG. 2] and instructions caches [262, 266, FIG. 2].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kim and Reader because they are both directed to the same multimedia processor, with each of the references claiming a different aspect of

the same multimedia processor. The combination of Kim with Reader, therefore, additionally teaches:

a data transfer switch [Kim: 280, FIG. 2] disposed within said multimedia processor and coupled to said second processor for transferring data to various modules [in particular Kim: 246, 262, 264, 266, 268, 270, FIG. 2] of said multimedia processor; and

a data streamer [246, FIG. 2] coupled to said data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within said multimedia processor, **at least one of which is a cache memory** [262, 264, 266, 268, 270, FIG. 2], in accordance with corresponding channel allocations.

The combination of Kim with Reader does not teach a multiplexer coupled to the interface for providing access between a selected number of I/O device driver units to external I/O devices via output pins.

Kusters teaches a method that uses a multiplexer [30, FIG. 1] coupled to a computer system [8, FIG.1] for providing access between a selected number of I/O device driver units [38a,..,38n, FIG.1] and external I/O devices [32a,..,32n] via output pins (parallel I/O port, Abstract).

Kusters further teaches the above method not being limited to any particular computer, single chip processor or apparatus; and also teaches a specialized apparatus to perform the methods above (col. 8, lines 4-14). Kusters, therefore, teaches a multiplexer being usable with a single chip processor; such multiplexer being either on the same chip as the processor, or external to the processor.

Kusters, therefore, teaches the claimed invention except for the particulars of the single chip processor, and except for a first host processor system coupled to the single chip processor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to couple Kusters' multiplexer to Reader's multimedia processor interface unit (such multiplexer being either internally or externally disposed on the multimedia processor) for the purpose of providing access between a selected number of I/O device driver units among a plurality of I/O device driver units to external devices via a limited number of output pins, such combination also enabling multiple devices to be used simultaneously for a same set of pins.

8. As per claims 20-25 and 27, Kusters teaches external I/O devices being controlled by a corresponding one of the I/O device driver units (Abstract: lines 11-12).

Reader teaches one of the external devices being a video decoder [Video A/D: Video Out, FIGs. 4, 5] and one the external devices being a video encoder [Video A/D: Video In, FIGs. 4, 5], with NTSC encoder/decoder being well known in the art at the time the invention was made for video encoders and decoders;

one of the external devices being a modem [MSP, FIG. 7]; with a transport channel interface being well known in the art at the time the invention was made for modems; and

three dimensional graphic signal [DirectX (3D), FIG. 7]; and an audio CODEC [114, FIG. 1].

9. As per claim 26, the combination above does not teach one of the external devices being an ISDN interface. It would have been obvious to one of ordinary skill in the art at the time the invention was made that ISDN represents one of the design choices for an external I/O device for the purpose of communicating data between the multimedia processor and other communications media.

10. As per claims 28-36, see the rejections to claims 19-27 above.

11. Claims 19-36 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over **Reader et al. (U. S. Pat. No. 6,192,073)** in view of **Kim (U. S. Pat. No. 5,926,187)**. The rejections to claims 19-36 above are incorporated by reference.

12. As per claim 19, Kim further teaches a multiplexer [515, FIG. 5] coupled to the interface unit [251, FIG. 1] for providing access between a selected number of I/O device driver units (col. 6, line 30-col. 7, line 8) to external I/O devices [110, 130, 150, FIG. 1] via output pins (col. 6, lines 10-29).

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to combine Kim and Reader because they are both directed to the same multimedia processor, with each of the references claiming a different aspect of the same multimedia processor, and because Kim's aforementioned teachings would allow the multiplexer to implement protocol for accessing different devices.

13. As per claims 20-36, Kim further teaches external I/O devices being controlled by a corresponding one of said I/O device driver units (col. 6, line 30-col. 7, line 8); one of the external devices being a NTSC decoder [col. 3, lines 7-8; 110, FIG. 1] and one the external devices being a NTSC encoder [col. 3, lines 7-8, 130, FIG. 1]; one of the external devices being an audio CODEC [150, FIG.1]; modem communications (col. 3, line 11) and modem software to demodulate data (col. 3, lines 45-47).

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claims 19-36 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 09/172,286, now U.S. Patent No. 6,347,344. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of the claims in the instant application are disclosed in claims 1-18 of the copending application.

Response to Arguments

16. Applicant's arguments filed 01/13/03 with respect to the 112 and 132 rejections have been fully considered but they are not persuasive. The processors [102, 104, 106, FIG. 1A] cited by applicant are processors disposed within the multimedia processor, hence are local processors and, do not constitute a first host processor system coupled to said multimedia processor.

17. Applicant's arguments with respect to claims 19-36 reciting a cache memory employed as a data transfer object of the data streamer have been considered and fully addressed with the new ground(s) of rejection.

18. Applicant's arguments with respect to the limitation for the data streamer performing DMA transfer among a plurality of modules is not persuasive because such limitation is not recited in claims 19-36. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further, even if the above limitation is recited in the claims, such limitation is directed to a manner that is well known in the art for transferring data from a source to a destination.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (703) 305-0138, and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7238 for After Final, (703) 746-7239 for Official, (703) 746-7240 for Customer Services, or (703) 746-5672 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Mail responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

Faxes for formal communications intended for entry should be sent to:

(703) 308-9051,

Hand-delivered responses should be brought to:

Crystal Park II, 2121 Crystal Drive, Arlington, Va, Fourth Floor

(Receptionist).

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TQN

January 16, 2003